Homework 11

1. A. Add Hamming parity bits to the value 204, assuming it is stored in unsigned format using 8 bits. \((1100\overline{1}1010100)\)

   B. Describe the data-recovery process and the exact value recovered if bit 3 is somehow flipped. Do the same if bit 9 is flipped, and if both 3 and 9 are flipped simultaneously. \((recovered \ to \ 204; \ recovered \ to \ 204; \ unrecoverable)\)

2. For each of the following sets of 8 data bits interleaved with 5 parity bits using the Hamming system, is the value valid, or was there an error? If the original unsigned number is recoverable, what is it? If not, why isn’t it?

   A. \(1101011101111\) (error; 255)

   B. \(1000100011111\) (valid; 129)

   C. \(1000000101111\) (error; unrecoverable)

3. Answer the questions for each MIPS processor in this table, whose stages have the latencies shown.

<table>
<thead>
<tr>
<th>P1</th>
<th>IF</th>
<th>ID</th>
<th>EX</th>
<th>MEM</th>
<th>WB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>300 ps</td>
<td>400 ps</td>
<td>350 ps</td>
<td>500 ps</td>
<td>100 ps</td>
</tr>
<tr>
<td>P2</td>
<td>200 ps</td>
<td>150 ps</td>
<td>120 ps</td>
<td>190 ps</td>
<td>140 ps</td>
</tr>
</tbody>
</table>

   A. How long will a clock cycle be, in both a pipelined and nonpipelined system? \((500 \text{ ps, } 1650 \text{ ps}; 200 \text{ ps, } 800 \text{ ps})\)

   B. What will the total latency of a \(lw\) instruction be, in both a pipelined and nonpipelined system? \((2500 \text{ ps, } 1650 \text{ ps}; 1000 \text{ ps, } 800 \text{ ps})\)

   C. If one could split any single stage into two new stages (each with half the latency) which stage should be split and what would the new period of the processor be, assuming a pipelined system? What would the total latency of \(lw\) be? \((MEM, 400 \text{ ps, } 2400 \text{ ps}; IF, 190 \text{ ps, } 1140 \text{ ps})\)

4. For the following questions, consider the MIPS code on the right. Assume that each of these instructions is divided into five stages (IF, ID, EX, MEM, and WB), and that each stage takes exactly one cycle to complete.

   A. How many cycles will it take to execute this code, assuming that the system is not pipelined? \((30 \text{ cycles})\)

   B. How many cycles will it take, assuming that the system is pipelined, but cannot support forwarding? \((16 \text{ cycles})\)

   C. How many cycles will it take, assuming that the system is pipelined, and allows forwarding? \((11 \text{ cycles})\)

   D. How many cycles will it take, assuming that the system is pipelined, allows forwarding, and a good compiler has optimized this code (reordering instructions)? \((10 \text{ cycles})\)

\[
\begin{align*}
\text{l}w & \quad \$t1, \ 0(\$s0) \\
\text{l}w & \quad \$t2, \ 4(\$s0) \\
\text{add} & \quad \$t3, \ \$t1, \ \$t2 \\
\text{s}w & \quad \$t3, \ 0(\$s0) \\
\text{s}ub & \quad \$t4, \ \$s4, \ \$t3 \\
\text{l}w & \quad \$t5, \ 0(\$s1)
\end{align*}
\]