

Homework 2

1. Answer the following questions for three different processors P1, P2, and P3, as shown in this table. The three execute the same instruction set, with the clock rates and CPIs shown.

	Clock Rate	CPI
P1	2 GHz	1.5
P2	1.5 GHz	1.0
P3	3 GHz	2.5

- A. Which processor has the highest performance? (*P2*)
- B. If each processor executes a program in 10 seconds, find the number of cycles and instructions. (*13.33 Ginst, 20 Gcyc; 15 Ginst, 15 Gcyc; 12 Ginst, 30 Gcyc*)
- C. We are trying to reduce time taken on a program by 30%. A certain technique can increase the clock rate, but results in 20% greater CPI. What clock rate needs to be obtained to make this trade-off worthwhile? (*3.43 GHz; 2.57 GHz; 5.14 GHz*)

2. Answer the following questions for three different processors running three different programs, as shown in this table.

	Clock Rate	# Instruc	Time
P1	2 GHz	20×10^9	7 s
P2	1.5 GHz	30×10^9	10 s
P3	3 GHz	90×10^9	9 s

- A. What is the instructions per cycle for each processor? (*1.43 inst/cyc; 2 inst/cyc; 3.33 inst/cyc*)
- B. What clock rate would P2 need, to reduce its execution time to that of P1? (*2.14 GHz*)
- C. What number of instructions would P2's program need, to run as fast as the one on P3? (*27 Ginst*)

3. Two different processors run the same assembly language. Each has a different clock rate. This language has four kinds of instructions: arithmetic, store, load, and branch instructions, each with a different CPI.

	Clock Rate	Arith CPI	Store CPI	Load CPI	Branch CPI
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

- A. A certain program has a million instructions divided as follows: 10% arithmetic, 20% store, 50% load, and 20% branch. Will P1 or P2 run it faster? (*P2*)
 - B. What is the overall CPI for this program on each processor? (*2.8 cyc/inst; 2 cyc/inst*)
 - C. How many clock cycles are required for the program on each processor? (*2.8 Mcyc; 2 Mcyc*)
4. A short program consists of 500 arithmetic instructions, 50 store instructions, 100 load instructions, and 50 branch instructions. Assume that arithmetic instructions take 1 cycle, load and store instructions take 5 cycles, and a branch takes 2 cycles.
- A. What is the execution time on a 2-GHz processor? (*675 ns*)
 - B. What is the program's CPI? (*1.93 cyc/inst*)

c. If the number of load instructions can be halved, what is the speed-up and the new CPI?
 ($1.23\times$; $1.69 \text{ }^{cyc}/_{inst}$)

5. Two different implementations of an assembly language (that has five different classes of instructions, A-E) are shown below:

	Clock Rate	CPI A	CPI B	CPI C	CPI D	CPI E
P1	1.0 GHz	1	2	3	4	3
P2	1.5 GHz	2	2	2	4	4

A. What is the possible *peak performance* of each processor, if it hits a stretch of fast instructions?
 ($1 \text{ }^{Ginst}/_s$; $0.75 \text{ }^{Ginst}/_s$)

B. Assume that there are equal numbers of instructions of each class, except those of class A which are twice as common as each of the others. Which computer is faster, and by how much? (*P2 is $1.31\times$ faster.*)

C. Assume that there are equal numbers of instructions of each class, except those of class E which are twice as common as each of the others. Which computer is faster, and by how much? (*P2 is $1.33\times$ faster.*)

6. A program consists of 1000 arithmetic instructions, 100 store instructions, 400 load instructions, and 50 branch instructions.

A. If arithmetic instructions take 1 cycle, loads and stores take 10, and branches take 3, what is the execution time on a 3-GHz processor? ($2.05 \mu s$)

B. If arithmetic instructions take 1 cycle, loads and stores take 2, and branches take 3, what is the execution time on a 3-GHz processor? ($0.717 \mu s$)

C. Assuming the cycles take the same number of instructions as in part b. What is the speed-up of the program if the number of arithmetic instructions can be halved? ($1.30\times$)

7. Let us say a manufacturing process makes 15-cm wafers. There are 90 dies in a wafer, and the process has a defect rate of 0.018 defects per cm^2 . Each wafer costs \$10 to manufacture.

A. What is the yield? (0.966)

B. What is the cost per working die? (11.5ϕ)

C. A variant process can increase the number of dies per wafer by 10%, at the cost of 15% more defects per area. What is the new (approximate) die area and yield? ($1.78 \text{ } cm^2$; 0.964)